Regulators ICs for Digital Cameras and Camcorders

System Switching Regulator ICs with Built-in FET (10V)

BD9739KN, BD9740KN

No.10036EAT07

●Description

The 7-channel switching regulators include built-in FETs, and are designed for use in digital still cameras. They feature built-in power FETs and soft start functionality, reducing the number of external components.

●Features

1) Wide supply voltage range: 1.5 V to 10 V
2) High-precision reference voltage: ± 1%
3) Built-in shutdown circuit for overload (timer-latch type)
4) Oscillator frequency is user-adjustable
5) Built-in thermal shutdown circuit
6) Standby mode current: 0 μA
7) Built-in load switch circuit
8) Selectable step-up/step-down mode
9) Supports inverting circuit for negative output voltage
10) Support a constant-current LED drive for backlight applications
11) Includes multiple synchronous rectification channels

●Applications

Digital still cameras, portable DVD players, and digital video cameras.

●Product lineup

Parameter	BD9739KN	BD9740KN
Input voltage	1.5 V to 10 V	1.5 V to 10 V
Reference voltage precision	1 V ± 1%	1 V ± 1%
Operating frequency range	100 k to 1.2 MHz	100 k to 1.2 MHz
Step-up	3CH	2CH
Step-down	2CH	1CH
Step-up/step-down switch regulator	1CH	3CH
Inverting	1CH	1CH
Built-in FET	3CH	1CH
Synchronous rectification	3CH	2CH
Load switching	3CH	—
Operating temperature range	-20℃ to +85℃	-20℃ to +85℃
Package	UQFN64	UQFN48

●Absolute maximum ratings

Parameter	Symbol	Ratings		Unit
		BD9739KN	BD9740KN	
Maximum supply voltage	VBAT,VCC,PVCC	-0.3 to +12	-0.3 to +12	V
	PVCCH,PVCCL	-0.3 to +15	-0.3 to +15	V
	DRAIN*H, DRAIN*L	-0.3 to +12	-0.3 to +12	V
	OUT1B	-0.3 to +20	-0.3 to +20	V
	OUT2B	-0.3 to +17	—	V
	SWOUT1,4,PGIN1,PG2,3	-0.3 to +12	—	V
	SWIN*	-0.3 to +20	—	V
Power dissipation	Pd	UQFN64	UQFN48	mW
		550 *1-2	500 *1-3	
		1000 *2-2	760 *2-3	
Operating temperature range	Topr	-25～+85		℃
Storage temperature range	Tstg	-55～+125		℃
Junction temperature	T_{jmax}	+125		℃

*1: IC without heat sink operation. Reduce by 5.5 mW/℃ (1-2), or 5.0 mW/℃ (1-3) when Ta ≥ 25℃.
*2: When mounted on a PCB (70 mm ×70 mm ×1.6 mm (thickness), glass epoxy).
Reduced by 10.0 mW/℃ (2-2), or 7.6 mW/℃ (2-3), when Ta ≥ 25℃.

●Recommended operating ranges

Parameter	Symbol	Ratings		Unit
		BD9739KN	BD9740KN	
Supply voltage	VBAT	1.5 to 10	1.5 to 10	V
	VCC, PVCC	1.5 to 10	2.8 to 10	V
	PVCCL, PVCCH	4.0 to 14	4.0 to 14	V

Parameter	Symbol	Ratings			Unit	Conditions
		Min.	Typ.	Max.		
[Oscillator]						
Oscillating frequency	f_{OSC}	0.1	—	1.2	MHz	
[Driver block]						
DRAIN pin input voltage	V_{DRAIN}	—	—	10	V	
N-channel FET output current (step-down)	I_{OFET1}	—	—	700	mA	
N-channel FET output current (step-up)	I_{OFET2}	—	—	300	mA	
LED channel output current	I_{OLED}	—	—	40	mA	
Driver output current	I_{OUT}	—	—	30	mA	External FET drive circuit
Driver peak current	I_{PEAK}	—	—	200	mA	External FET drive circuit
Startup NPN TR sink current	$I_{NPNSINK}$	—	—	500	mA	
[Positive/negative regulators]						
SWOUT1 pin sink current	I_{SWOUT1}	—	—	10	mA	
PGOUT1 pin source current	I_{PGOUT1}	—	—	100	mA	
PG23 pin sink current	I_{PG23}	—	—	1	mA	
SWOUT4 pin source current	I_{SWOUT4}	—	—	50	mA	(BD9739KN)
SWOUT6 pin source current	I_{SWOUT6}	—	—	50	mA	
SWOUT7 pin source current	I_{SWOUT7}	—	—	50	mA	

●Electrical characteristics

(Unless otherwise specified, Ta = 25℃, VBAT = 3 V, VCC = 5 V, RT = 11 kΩ, CT = 180 pF, STB1 to STB7 = 3 V)

Parameter		Symbol	Limits			Unit	Conditions
			Min.	Typ.	Max.		
[Reference voltage, reference voltage for inverting]							
Output voltage		V_{REF2}	0.99	1.0	1.01	V	
Line regulation		DV_{LI}	—	4.0	12.5	mV	VCC = 3.0 V to 9.5 V
Load regulation		DV_{LO}	—	1.0	7.5	mV	IREF = 10 μA to 100 μA
Output current when shorted		I_{OS}	0.2	1	—	mA	VREF = 0 V
[Internal regulator]							
Output voltage REGA		V_{REGA}	2.4	2.5	2.6	V	IREG = 1 mA
[Under voltage lockout circuit]							
Detection threshold voltage 1		V_{STD1}	3.45	3.6	3.75	V	PVCCL monitor
Hysteresis width 1		ΔV_{ST1}	—	300	—	mV	
Detection threshold voltage 2		V_{STD2}	2.3	2.4	2.5	V	VCC monitor
Hysteresis width 2		ΔV_{ST2}	—	200	—	mV	
Detection threshold voltage 3		V_{STD3}	—	2.0	—	V	VREGA monitor
Hysteresis width 3		ΔV_{ST3}	—	50	—	mV	
[Startup circuit block]							
Oscillating frequency		f_{START}	50	120	220	kHz	
Operation start VBAT voltage		V_{ST1}	1.5	—	—	V	VBAT pin monitor
Soft start charge current		I_{SS1}	1.1	2.2	3.3	μA	VSS1 = 0 V
[Short protection circuit]							
Timer threshold voltage		V_{TC}	2.1	2.2	2.3	V	FB pin monitor
SCP pin source current		I_{SCP}	0.5	1.0	1.5	μA	VSCP = 0.1 V
			2	4	6		(BD9740KN)
SCP pin detection voltage		V_{TSC}	0.45	0.50	0.55	V	
			0.9	1.0	1.1		(BD9740KN)
SCP pin standby voltage		V_{SSC}	—	22	170	mV	
[Triangular waveform oscillator]							
Oscillating frequency		f_{OSC1}	450	500	550	kHz	RT = 11 kΩ, CT = 180 pF
Frequency stability		Df	—	0.3	2	%	VCC = 3.0 V to 9.5 V
RT pin voltage		V_{RT}	0.78	1.00	1.22	V	
[Soft start 23 block] (BD9738KN, BD9739KN)							
Soft start charge current		I_{SS23}	5	10	15	μA	VSS23 = 0 V
[Error amp]							
Low-level output voltage		V_{OL}	—	1.3	—	V	INV = 2 V
High-level output voltage		V_{OH}	V_{REGA} - 0.3	—	—	V	INV = 0 V
Output sink current		I_{OI}	36	72	—	μA	FB = 1.7 V, VINV = 1.1 V
Output source current		I_{OO}	36	72	—	μA	FB = 1.7 V, VINV = 0.9 V
DTC pin upper resistance		R_{DTCU}	20	30	40	kΩ	(BD9740KN)
DTC pin lower resistance		R_{DTCD}	65	95	125	kΩ	(BD9740KN)
NON pin input range		I_{RES}	-0.3	-	1.5	V	
Non-inverted pin reference voltage		V_{NON7}	—	0.2	—	V	
[PWM comparator]							
Input threshold voltage		V_{T0}	—	1.49	—	V	0% duty
		V_{T100}	—	1.95	—	V	100% duty
MAX DUTY		D_{MAX1}	77	85	93	%	VINV = 0.9 V, VSCP = 0 V
MAX DUTY (step-up operation)		D_{MAX2}	77	85	93	%	VINV = 0.9 V, VSCP, UDSEL = 0 V
[Output circuit]							
High-level output voltage		V_{SATH}	V_{CC}-1.6	V_{CC}-0.8	—	V	IO = 30 mA
Low-level output voltage		V_{SATL}	—	0.8	1.6	V	IO = -30 mA
High-side N-channel FET on resistance		R_{ONH}	—	270	500	mΩ	PVCCH = 5 V(IO = 200 mA)
			—	300	500		(BD9740KN)
Low-side N-channel FET on resistance		R_{ONL}	—	270	500	mΩ	PVCCL = 5 V(IO = 200 mA)
			—	300	500		(BD9740KN)
CH7 N-channel FET on resistance		R_{ONL7}	—	0.7	1.4	Ω	PVCCL = 5 V(IO = 50 mA)
[Step-up/step-down selector]							
UDSEL pin control voltage	Step-down	V_{UDDO}	V_{CC} × 0.7	—	V_{CC}	V	
	Step-up	V_{UDUP}	0	—	V_{CC} × 0.3	V	

Note: This IC is not designed to be radiation-resistant.

(Unless otherwise specified, Ta = 25℃, VBAT = 3 V, VCC = 5 V, RT = 11 kΩ, CT = 180 pF, STB1 to STB7 = 3 V)

Parameter		Symbol	Limits			Unit	Conditions
			Min.	Typ.	Max.		
[Power on switching block] (BD9739KN)							
SWOUT1	Output voltage	V_{SAT}	—	0.1	0.3	V	IO = 1 mA
	Leak current	I_{LEAK}	—	0	5	μA	STB = 0 V
SWOUT4	Output voltage	V_{SAT}	—	0.1	0.3	V	IO = 100 μA
	Leak current	I_{LEAK}	—	0	5	μA	STB = 0 V
SWOUT4,6	Output voltage	V_{SAT}	V_{SWIN6} - 0.3	V_{SWIN6} - 0.1	—	V	IO = 20 mA VSWIN = 5 V
	Leak current	I_{LEAK}	—	0	5	μA	STB = 0 V
SWOUT7	Output voltage	V_{SAT}	V_{SWIN7} - 0.3	V_{SWIN7} - 0.1	—	V	IO = 10 mA VSWIN = 10 V
	Leak current	I_{LEAK}	—	0	5	μA	STB = 0 V
[Soft start block] (BD9740KN)							
Soft start time of CH4		T_{SS1}	1.8	3.6	6.0	msec	VCC = PVCC = 5V, PVCCH = 5.0V STB 0→3 V
Soft start time of CH2, 3		T_{SS2}	1.8	3.6	6.0	msec	VCC = PVCC = 5V, STB = 3 V INV4 = 0→1.2 V
CH2, CH3 soft start INV4 threshold voltage at start		V_{PG4}	0.72	0.80	0.88	V	VCC = PVCC = 5 V PVCCH = 5.0 V
[STB1 to STB7]							
STB pin control voltage	ON	V_{STBH}	2.0	—	11	V	STB
	OFF	V_{STBL}	-0.3	—	0.3	V	
STB pin pull-down resistance		R_{STB}	250	400	700	kΩ	STB
[Circuit current]							
Standby current 1 (VBAT pin sink current)		I_{STB1}	—	—	5	μA	STB1 to STB7 = 0 V
Standby current 2 (VCC, PVCC pin sink current)		I_{STB2}	—	—	5	μA	STB1 to STB7 = 0 V
Circuit current at startup (VBAT pin sink current)		I_{ST}	—	30	100	mA	CT = 1.7 V VCC = 0 V
Circuit current 1 (VBAT pin sink current)		I_{CC1}	—	100	300	μA	CT = 1.7 V
Circuit current 2 (VCC, PVCC pin sink current)		I_{CC2}	—	5	15	mA	CT = 1.7 V INV = 2.5 V

Note: This IC is not designed to be radiation-resistant.

●PVCCH and PVCCL input voltages

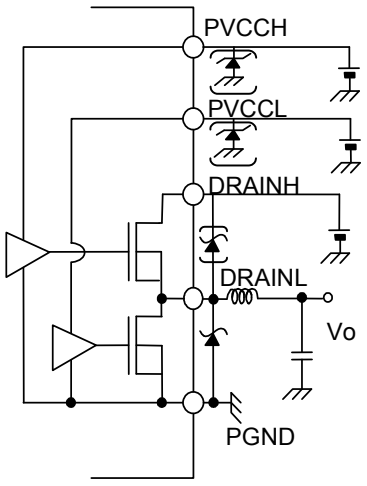


Fig. 1 Synchronous Rectification Channel with Built-In FET

- Synchronous rectification channels with built-in FETs include, N-channel FETs for both the high-side and low-side configuration. The driver block's power source is supplied to the PVCCL pin for the low-side and the PVCCH pin for the high-side. (For the BD9740KN, both sides are supplied to the PVCCH pin.) In order to turn the FET on, a potential of at least 4 V must be supplied to the PVCCL pin, and a potential of at least, DRAINH pin voltage + 4 V, must be supplied to the PVCCH pin.

Note:

- The breakdown voltage for the PVCCL and PVCCH pins is 15 V. For applications that with voltages exceeding 15 V, add a zener diode, or other components, to provide overvoltage protection.
- Shorting the DRAINH pin with the ground, while a charge remains in the output capacitor, may cause unexpected current flow, resulting in damage to the IC. Add an external protective diode for applications where this possibility exists.

●Block diagram and application circuit (BD9739KN)

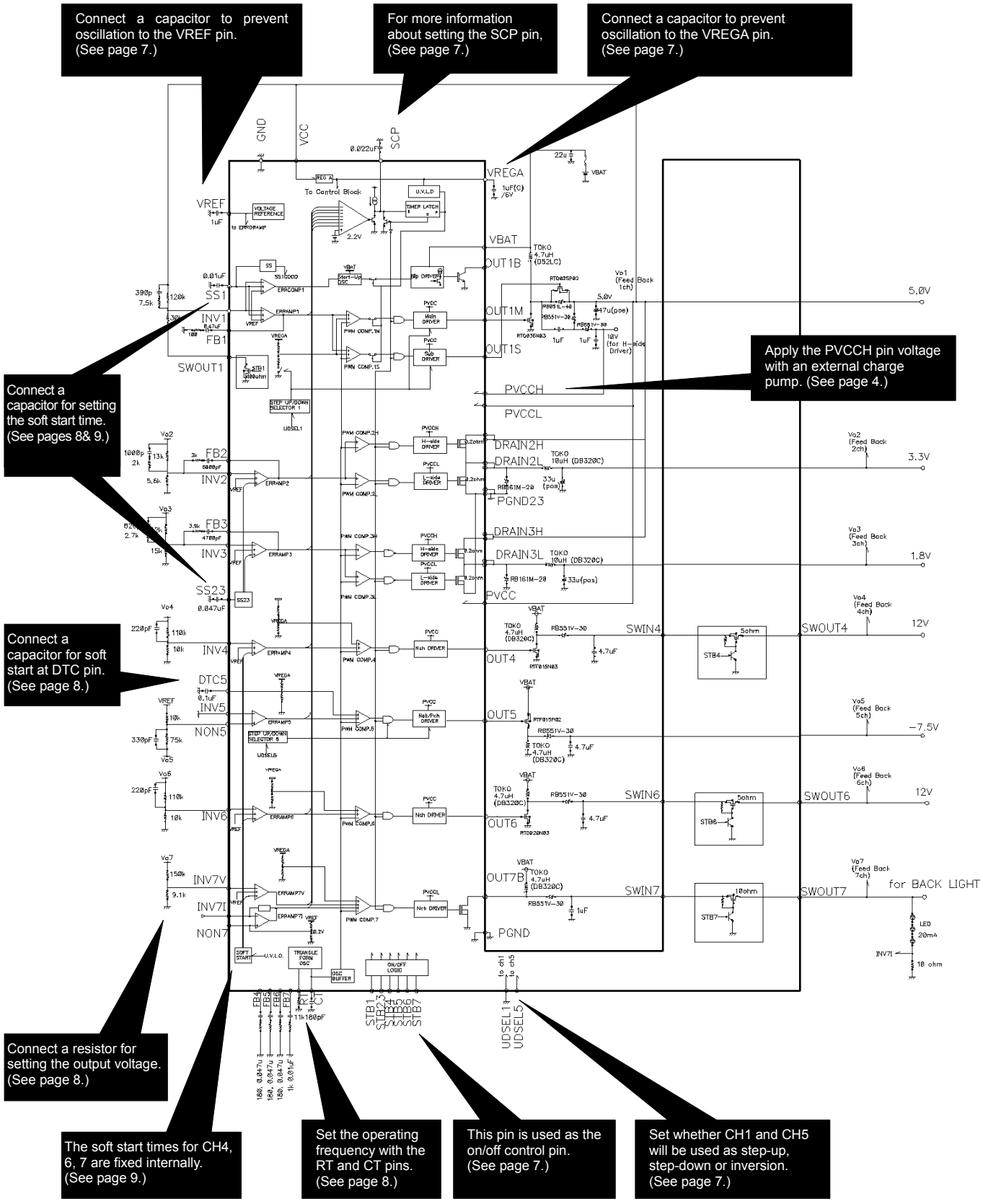


Fig. 2 BD9739KN Application Circuit

●Block diagram and application circuit (2) BD9740KN

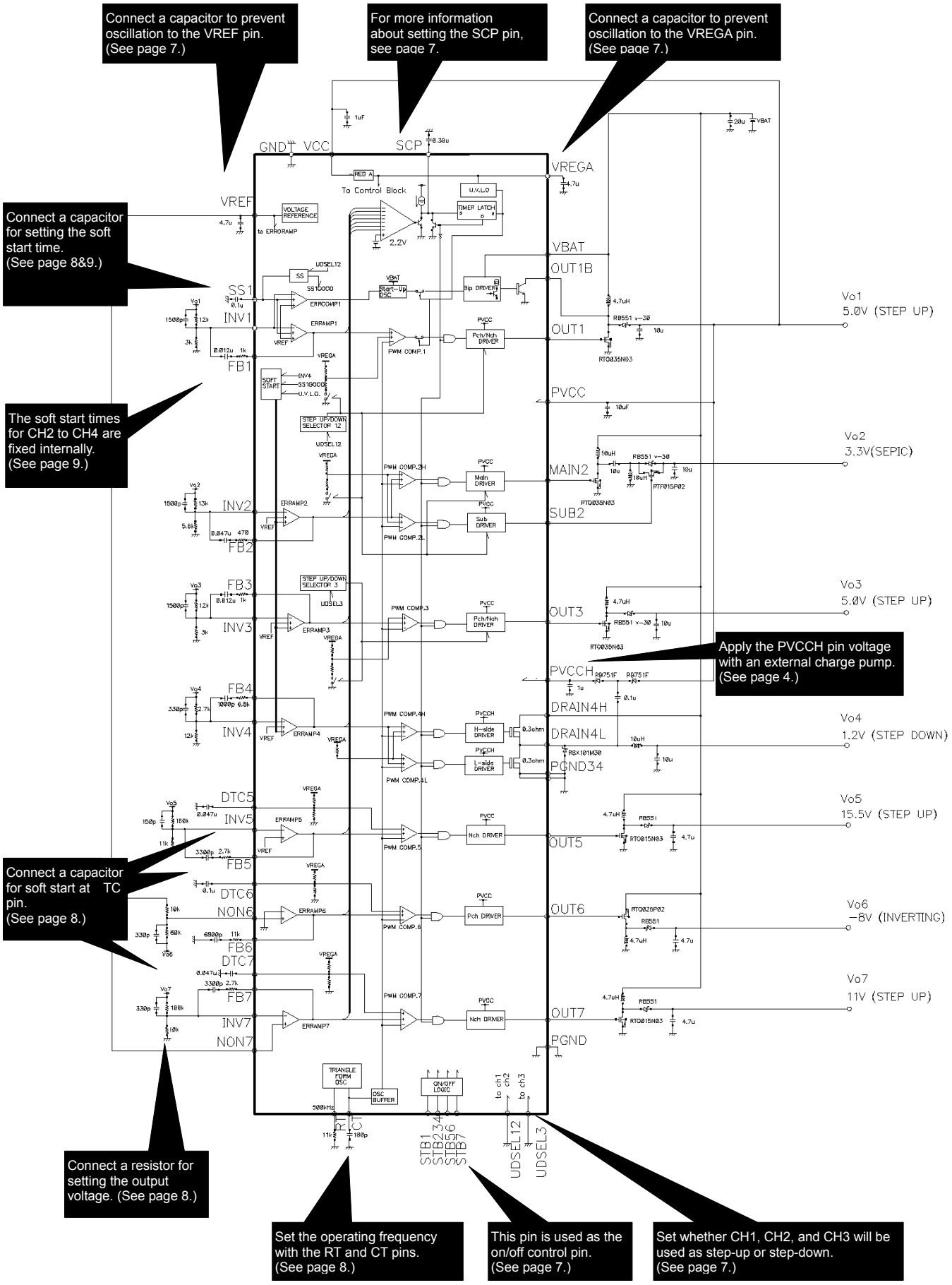


Fig. 3 BD9740KN Application Circuit

●BD9739KN Pin No.

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
61	VBAT	60	OUT1B	44,36	NON5,7
29	VCC	4,5,12,13	DRAIN2,3H	28	SS1
54	PVCC	6,7,10,11	DRAIN2,3L	25	SS23
14	PVCCH	55	OUT1M	34	RT
59	PVCCL	56	OUT1S	33	CT
8,9,57	PGND23,PGND	35	VREF	32	SCP
42	GND	43	DTC 5	1,64	UDSEL1,5
30	VREGA	26,24,21,47,46,41,39	FB 1～7	15,16,17,18,19,20	STB 1,23,4,5,6,7
51,52,53	OUT4,5,6	27,23,22,48,45,40	INV 1～6	50,2,62	SWIN4,6,7
58	OUT7B	37,38	INV7I,INV7V	31,49,3,63	SWOUT 1,4,6,7

●BD9740KN Pin No.

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
4	VBAT	44	MAIN2	30,37	NON6,NON7
21	VCC	43	SUB2	17	SS1
46	PVCC	5	OUT1B	23	RT
10	PVCCH	9	DRAIN4H	24	CT
42	PGND	8	DRAIN4L	25	SCP
6,7	PGND4	20	VREF	1	UDSEL12
31	GND	3,38,39	DTC 5～7	2	UDSEL3
22	VREGA	16,18,27,28,32,35,36	FB 1～7	11,12,13,14	STB1,234,56,7
40,41,45,47,48	OUT1,3,5,6,7	15,19,26,29,33,34	INV 1～5,7		

●Block diagram explanation and setting peripheral IC components

1. Voltage reference (VREF)
   VREF is the reference voltage source of 1.0V output voltage.
   Connect a capacitor to prevent oscillation. Set the capacitance from 1.0 μF to 10 μF.

2. REGA
   REGA and REGD are regulators with output voltages of 2.5 V. REGA is used as the power supply for the IC's internal blocks.Connect a capacitor to prevent oscillation. Set the capacitance from 4.7 μ to 10 μF.

3. UDSEL
   To enable step-up mode, connect VCC to the UDSEL pin. To enable step-up mode connect 0V to the UDSEL pin.
   When using the startup circuit, set the pin to step-up mode. Because the pin uses COMS inverter input, you must connect the pin to either GND or VCC in order to prevent undefined input.

4. On/off logic
   The voltage applied to the STB pins can be controlled whether each channel is on or off.
   CH1, CH4, and CH5 can be controlled independently, while CH2 and CH3 can be controlled simultaneously.
   Applying a voltage of over 2 V turns on the corresponding channel(s), while leaving the pin open or applying 0 V turns off the corresponding channel(s).
   Turning off all channels causes the IC to be in a standby state.
   Each pin is connected to GND by a 400 kΩ pull-down resistor.

5. Setting the short protection detection time
   The detection time can be set when the capacitor is connected to the SCP pin.
   When the detection time is reached, the latch circuit operates, turning off the output for all channels.
   To reset the latch circuit, turn all STB pins off, and then back on again.
   Detection time (sec) = CSCP × VTSC / ISCP
   (CSCP: capacitance; VTSC: SCP pin detection voltage, ISCP: SCP pin source current)
   *Set the capacitor that is connected to the SCP pin from 0.001 μF to 2.2 μF.

6. Setting the oscillating frequency

The oscillating frequency can be set by connecting the resistance value to the RT pin and connecting the capacitance value to the CT pin.

Oscillating frequency = VRT / (CT × RT) (Unit: Hz)

*Set the resistance value, connected to the RT pin, from 4.7 kΩ to 30 kΩ

*Set the capacitance value, connected to the CT pin, from 100 pF to 10,000 pF.

(VRT: RT pin voltage; CT: OSC timing capacitance; RT: OSC timing resistance)

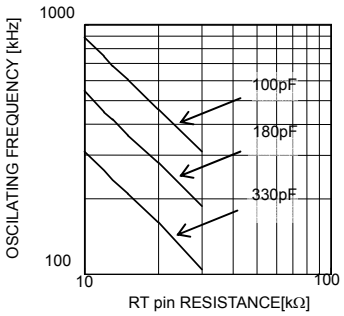


Fig. 4 Oscillating Frequency Versus RT Pin Resistance

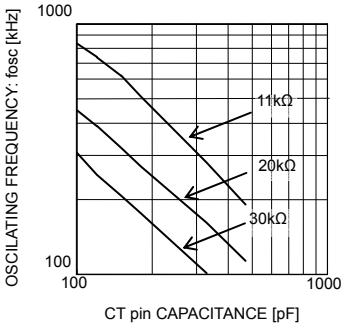


Fig. 5 Oscillating Frequency Versus CT Pin Capacitance

7. Startup channel soft-start operation

The startup channel's soft start can be controlled by the capacitor connected to the SS1 pin.

Times can be determined with the following equation:

Startup time (sec) = (VSS / ISS) × CSS

(VSS = SS pin voltage [= 0.7 V], ISS = soft start charge current [= approximately 2.0 μA]; CSS = capacitor capacitance)

Example: When CSS = 0.01 μF, startup time = 0.7 / (2.0 ×10-6) × (0.01 × 10-6) = 3.5 ms

*Set the capacitance value, connected to the SS1 pin, from 0.001 μF to 2.2 μF.

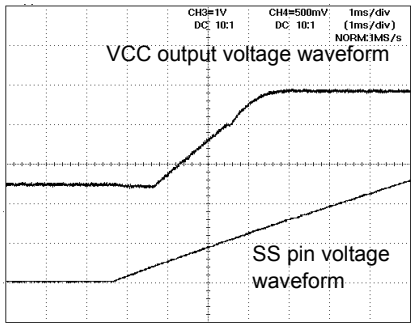


Fig. 6 Startup Channel Startup Waveform (Reference Data)

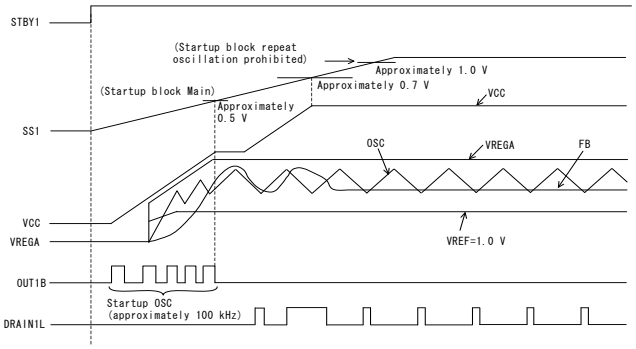


Fig. 7 Timing Chart

8. SWOUT1 pin (BD9734KN/BD9738KN/BD9739KN)

To prevent current from flowing from VOUT1 to the feedback resistor, during standby operation, connect the ground side of CH1's feedback resistor to SWOUT1.

9. Soft start operation depending on SS pins (BD9739KN)

Soft start operation for CH2 and CH3 can be controlled by the capacitor connected to the SS23 pins.

Times can be determined with the following equation:Startup time (sec) = (VSS / ISS) × CSS23

(VSS: SS pin voltage [= 1.0 V]; ISS: soft start charge current [= approximately 10 μA]; CSS: capacitance)

*Startup of CH2 begins when CH3 output reaches approximately 70%.

*Set the capacitance value, connected to each SS23 pin, from 0.005 μF to 1.0 μF.

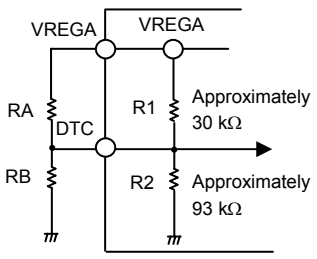


Fig. 8 DTC External Setting Circuit

10. Setting MAX DUTY
The DTC voltage is determined by the internal R1 and R2 resistance values. The DTC voltage can be changed by connecting resistance values that are from 1 to 2 digits smaller than the internal R1 (30 kΩ) and R2 (93 kΩ) resistors, to the RA and RB pins.
*The resistors connected to the RA and RB pins should be at least 5 kΩ. Avoid shorting the VREGA and DTC pins.
*When VCC falls to 2.8 V or below, a protection circuit will operate to limit MAX DUTY in order to prevent the IC from malfunctioning when VREGA (the internal circuit power supply) drops.

11. Soft start operation triggered by the DTC pin
Soft start operation can be set by connecting a capacitor to the DTC pin. Setting the STBY pin to high will cause the capacitor connected to the DTC pin to be charged by the internal pull-up resistor.
Startup will begin when this voltage reaches the minimum voltage of the CT pin's triangular waveform.
*Set the capacitance connected to each DTC pin to 10 μF or less.

12. Internal soft start operation
Soft start times are set internally for CH4, CH6, and CH7 (BD9739KN); and CH2 to CH4 (BD9740KN).
BD9739KN CH4, 6, 7: 2.7 ms
BD9740KN CH2 to CH4: 3.6 ms
(Soft start operation of CH2 and CH3 is delayed until CH4 reaches approximately 80%.)

13. Setting the error amp feedback resistance
(1) Feedback resistance order (BD9739KN, BD9740KN)
Error amp differential input is formed by a PNP transistor, with the base current of this input flowing into the lower voltage divider resistor. In the worst case, this current may reach 0.2 μA. For this reason, when the resistance of the lower resistor is increased, the base current may cause an error in the output voltage. For example, resistance values of 40 kΩ, 20 kΩ, and 10 kΩ result in errors of 1%, 0.5%, and 0.25%, respectively. Refer to these values when setting the resistance value.
(2) Setting the inverted channel (BD9739KN, BD9740KN)
For the BD9739KN, connect the CH5 error amp reference voltage (INV5) to the ground.
For the BD9740KN, the CH6 error amp reference voltage is grounded internally.
*It is recommended to use a 10 kΩ resistor between VREF and CH5 output. Use a resistance value from 5 kΩ to 20 kΩ.

●I/O Equivalent circuit diagrams

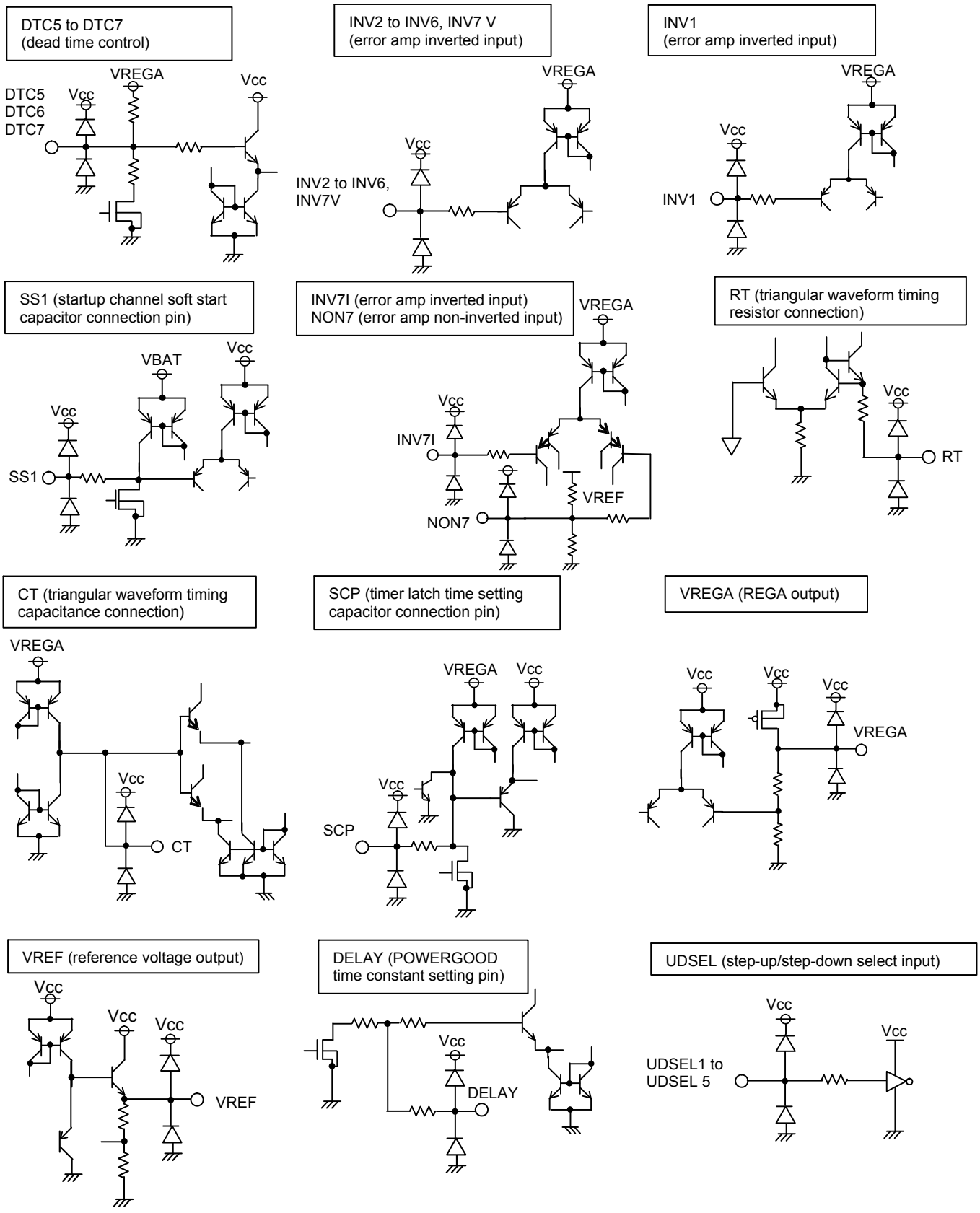
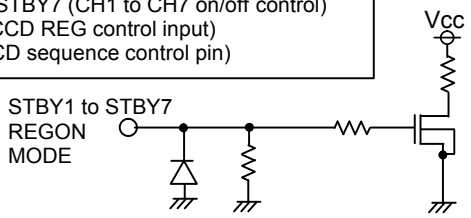
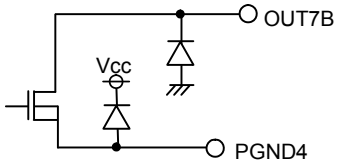


Fig. 9 I/O Equivalent Circuit Diagrams (1)

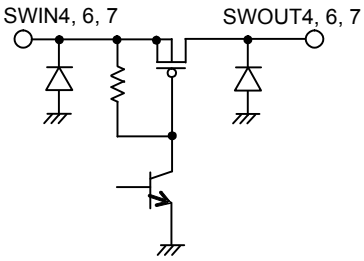
STBY1 to STBY7 (CH1 to CH7 on/off control)
REGON (CCD REG control input)
MODE (CCD sequence control pin)



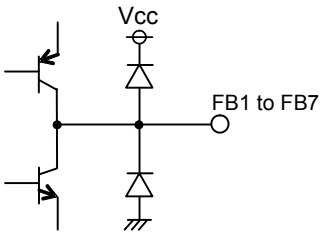
7CH (power transistor drain output)



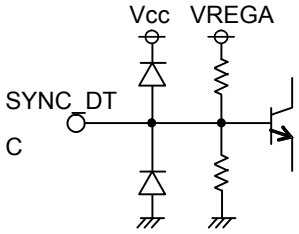
SWIN (load switch input pin)
SWOUT (load switch output pin)



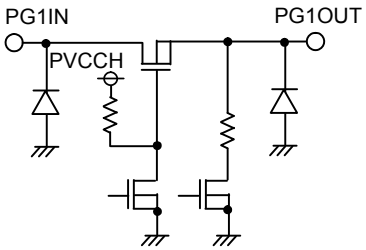
FB (error amp output)



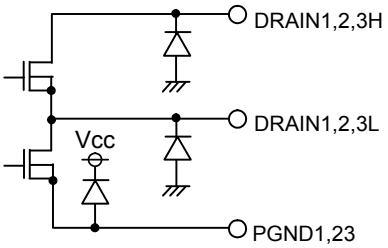
SYNC_DTC (synchronous rectification delay time setting pin)



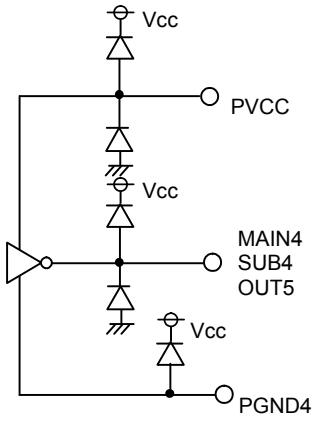
PG1IN (POWERGOOD 1 input)
PG1OUT (POWERGOOD switch 1 output)



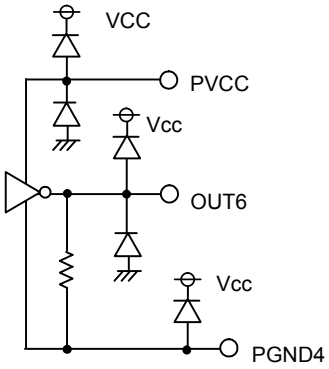
DRAIN1, 2, 3H
(power MOS drain for CH1, CH2, and CH3)
DRAIN1, 2, 3L
(power MOS drain for CH1, CH2, and CH3)
PGND1, 23 (output step ground)



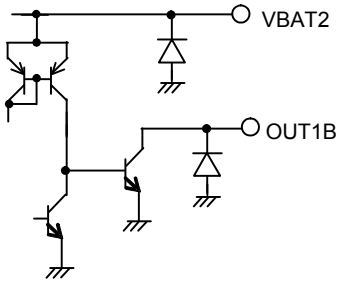
MAIN4 (CH4 main output)
SUB4 (CH4 sub output)
OUT5 (power transistor connection)



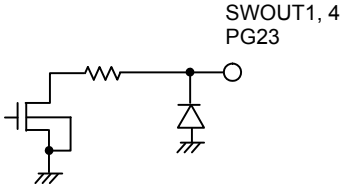
OUT6 (power transistor connection)
PVCC (power supply input)
PGND4 (power ground)



VBAT2 (battery input [driver block])
OUT1B (CH1 power transistor collector output)



SWOUT1, 4 (load switch output pin)
PG23 (POWERGOOD switch 23 output)



SS2 (soft start capacitor connection pin)

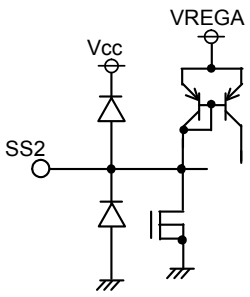


Fig. 10 I/O Equivalent Circuit Diagrams (2)

●Notes for use

1) Absolute maximum ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2) Reverse polarity connection of the power supply
Connecting the of power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

3) Power supply lines
Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, note that capacitance characteristic values are reduced at low temperatures.

4) GND voltage
Ground-GND potential should maintain at the minimum ground voltage level. Furthermore, no terminals should be lower than the GND potential voltage including an electric transients.

5) Thermal design
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

6) Inter-pin shorts and mounting errors
Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if positive and ground power supply terminals are reversed. The IC may also be damaged if pins are shorted together or are shorted to other circuit's power lines.

7) Operation in a strong electromagnetic field
Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

8) ASO
When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

9) Thermal shutdown circuit (TSD circuit)
The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

10) Capacitors connected between output and ground pins
If a large capacitance value is connected between the output and ground pins, and if the VCC falls to 0 V or becomes shorted with the ground pin, the current stored in the capacitor may flow to the output pin. This can cause damage to the IC. Set capacitors connected between the output and ground pins to values that fall within the recommended range.

11) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to, or removing it from a jig or fixture, during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting and storing the IC.

12) Regarding input pin of the IC (Fig 11)
This monolithic IC contains P^+ isolation and P substrate layers between adjacent elements to keep them isolated. P–N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:
When GND > Pin A and GND > Pin B, the P–N junction operates as a parasitic diode.
When Pin B > GND > Pin A, the P–N junction operates as a parasitic transistor.
Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

13) Ground wiring patterns
The power supply and ground lines must be as short and thick as possible to reduce line impedance. Fluctuating voltage on the power ground line may damage the device.

14) STB pin voltage
Set the STB pin voltage to 0.3 V or lower when setting channels to a standby state, or to 2.0 V or higher when setting channels to an operational state. Do not lengthen transition times or fix the STB pin voltage to values higher than 0.3 V or lower than 2.0 V. Doing so may cause the IC to malfunction.

15) Common supply voltage
Use a common supply voltage for both the driver block and the main block. The IC is not compatible with applications requiring the driver block to be used while applying user-selected voltages.

16) Setting the MAX DUTY
MAX DUTY limitations may not operate when using the IC at high frequencies. When using the IC in such applications, allow for sufficient margins when setting external components.

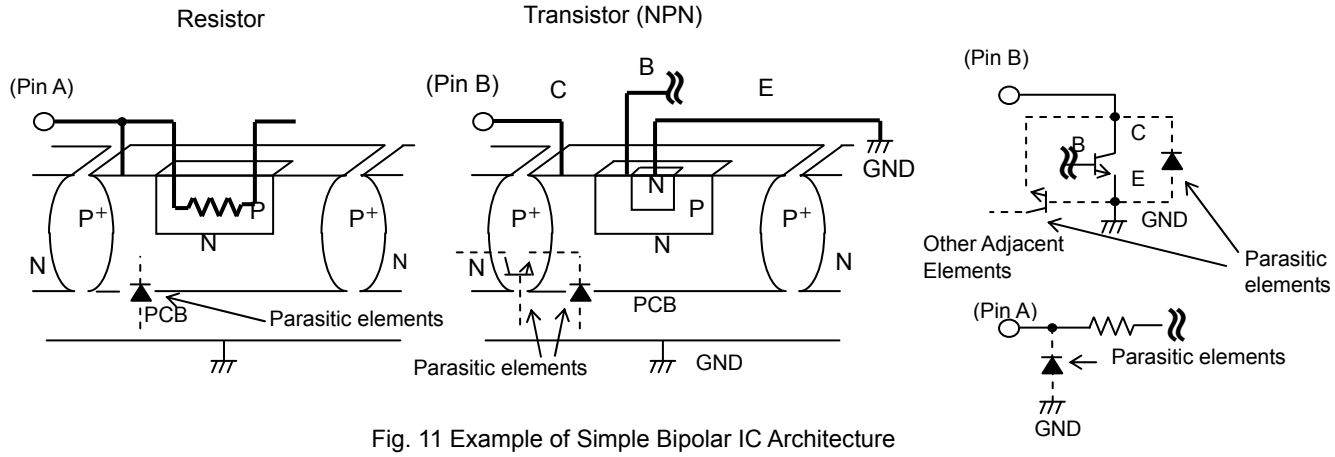


Fig. 11 Example of Simple Bipolar IC Architecture

●Ordering part number

B	D	9	7	3	9	K	N	-	E	2

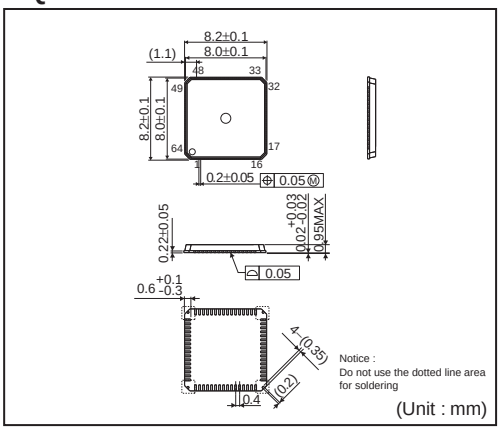
Part No.

Part No.
9739
9740

Package
KN: UQFN64
UQFN48

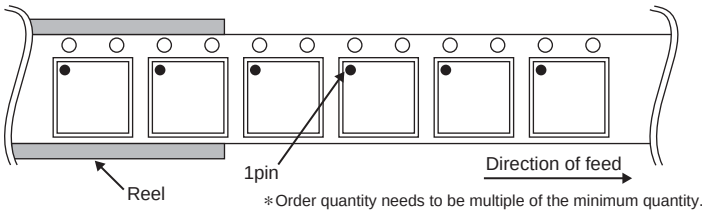
Packaging and forming specification
E2: Embossed tape and reel

UQFN64



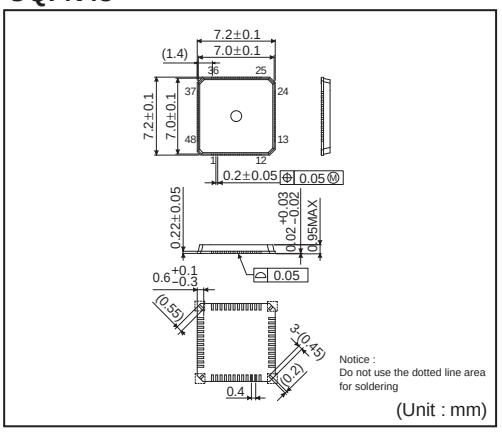
<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



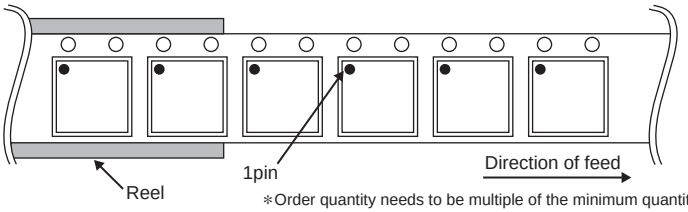
∗Order quantity needs to be multiple of the minimum quantity.

UQFN48



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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