Ordering number : ENA1192

SANYO Semiconductors
DATA SHEET

LV8053LG — Bi-CMOS LSI For Digital Still Camera 7-channel Single-chip Motor Driver IC

Overview

LV8053LG is a 7-channel single-chip motor driver IC for digital cameras.

Features

- 6 PWM drive forward/reverse motor driver channels
- One constant current forward/reverse motor driver channel

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VM max		6	V
	V_{CC} max		6	V
Output transisror voltage between drain and source	V_{DS} max		7	V
Output current	I_O max	Channels 1 to 7	800	mA
Allowable power dissipation	Pd max	Mounted on a specified board. *	1.6	W
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* Specified circuit board : 50mm×40mm×0.8mm, glass epoxy four-layer board.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	VM		2.7 to 5.5	V
	V_{CC}		2.7 to 5.5	V
Logic input voltage	V_{IN}		0 to V_{CC}+0.3	V
VLIM pin input voltage	VLIM		0 to V_{CC}-1.6	V

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Electrical Characteristics at Ta = 25°C, VM = 5V, V_{CC} = 2.8V, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Standby mode current drain	Istn	PS = "L"			1.0	μA
VM current drain	IM	PS = "H", EN = "H", with no load IM1+IM2+IM3		100	300	μA
V_{CC} current drain	I_{CC}	PS = "H", EN = "H", with no load			2.0	mA
V_{CC} low-voltage cutoff voltage	VthV_{CC}		1.0	1.8	2.4	V
Low-voltage hysteresis voltage	VthHIS		100		200	mV
Thermal shutdown temperature	TSD	Design guarantee value *	140	160	180	°C
Thermal hysteresis width	ΔTSD	Design guarantee value *	5	10	20	°C
Output on-resistance	Ron1	Ta = 25°C, I_O = 800mA, VM = 5V Upper side+lower side, channels 1 to 6			1.5	Ω
	Ron2	Ta = 25°C, I_O = 400mA, VM = 3V Upper side+lower side, channels 1 to 6		1.65	2.0	Ω
	Ron3	Ta = 25°C, I_O = 800mA, VM = 5V Upper side+lower side, SENSE = 0V, channel 7			1.25	Ω
	Ron4	Ta = 25°C, I_O = 800mA, VM = 5V Upper side+lower side, SENSE = 0.15V, channel 7			1.28	Ω
	Ron5	Ta = 25°C, I_O = 800mA, VM = 5V Upper side+lower side, SENSE = 0.75V, channel 7			1.34	Ω
	Ron6	Ta = 25°C, I_O = 400mA, VM = 3V Upper side+lower side, SENSE = 0V, channel 7		1.45	1.8	Ω
Output leakage current	$I_O$leak				1	μA
Diode forward voltage	VD	ID = -800mA			1.2	V
Output current	Iout1	Channel 7, VLIM = 0.25V, RNF = 2.5Ω, RM = 5Ω	97	100	103	mA
	Iout2	Channel 7, VLIM = 0.30V, RNF = 1.0Ω, RM = 5Ω	291	300	309	mA
Logic pin internal pull-down resistance	Rin	Applied to all logic input pins	50	100	200	kΩ
Logic pin input current	IinL	V_{IN} = 0V, applied to all logic input pins			1.0	μA
	IinH	V_{IN} = 2.8V, applied to all logic input pins	15	30	50	μA
Logic input high-level voltage	VinH	Applied to all logic input pins	V_{CC}×0.7		V_{CC}	V
Logic input low-level voltage	VinL	Applied to all logic input pins	0		V_{CC}×0.3	V
VREF voltage	Vref1	Iref = 0mA	0.84	0.9	0.96	V
	Vref2	Iref = 1mA (source)	0.84	0.9	0.96	V
	Vref3	Iref = -100μA (sink)	0.84	0.9	0.96	V
Turn-on time	Ton1	V_{CC} = 2.7V, VM = 4.7V, RM = 50Ω, channels 1 to 6 (Note 1)		0.5	2.0	μs
	Ton2	V_{CC} = 2.7V, VM = 4.7V, RM = 50Ω, channel 7 upper side (Note 1, test circuit 1)		0.5	2.0	μs
	Ton3	V_{CC} = 2.7V, VM = 4.7V, VLIM = 0.3V, RNF = 2.0Ω, RM = 5Ω, channel 7 lower side (Note 1, test circuit 2)		0.5	13.0	μs
Turn-off time	Toff1	V_{CC} = 2.7V, VM = 4.7V, RM = 50Ω, channels 1 to 6 (Note 2)		0.1	0.5	μs
	Toff2	V_{CC} = 2.7V, VM = 4.7V, RM = 50Ω, channel 7 upper side (Note 2, test circuit 1)		0.1	0.5	μs
	Toff3	V_{CC} = 2.7V, VM = 4.7V, VLIM = 0.3V, RNF = 2.0Ω, RM = 5Ω, channel 7 lower side (Note 2, test circuit 2)		0.05	2.0	μs

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Rising time	Tr1	V_{CC} = 2.7V, VM = 4.7V, RM = 50Ω, channels 1 to 6 (Note 1)	0.1	0.3	1.0	μs
	Tr2	V_{CC} = 2.7V, VM = 4.7V, RM = 50Ω, channel 7 upper side (Note 1, test circuit 1)	0.1	0.3	1.0	μs
	Tr3	V_{CC} = 2.7V, VM = 4.7V, VLIM = 0.3V, RNF = 2.0Ω, RM = 5Ω, channel 7 lower side (Note 1, test circuit 2)	0.5	4.0	9.0	μs
Falling time	Tf1	V_{CC} = 2.7V, VM = 4.7V, RM = 50Ω, channels 1 to 6 (Note 2)		0.05	0.2	μs
	Tf2	V_{CC} = 2.7V, VM = 4.7V, RM = 50Ω, channel 7 upper side (Note 2, test circuit 1)		0.05	0.2	μs
	Tf3	V_{CC} = 2.7V, VM = 4.7V, VLIM = 0.3V, RNF = 2.0Ω, RM = 5Ω, channel 7 lower side (Note 2, test circuit 2)		0.03	1.0	μs

* Design guaranteed value (No measurement is performed.)

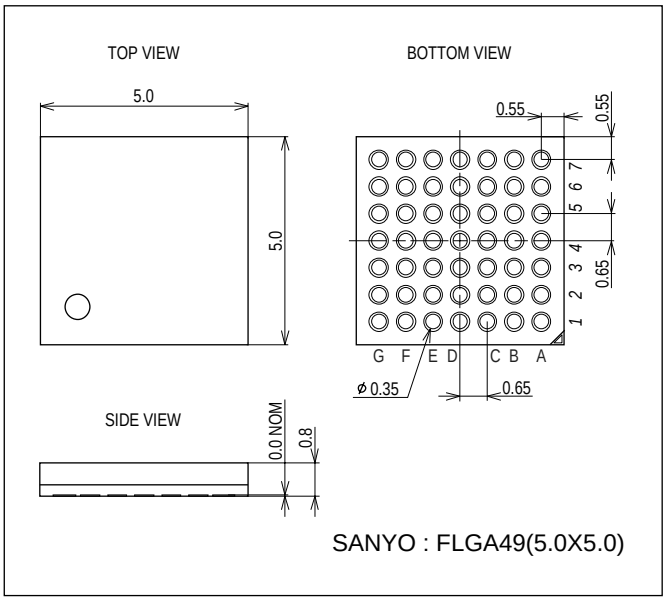
Note 1 : Time from the edge at which the control input switches (0.5×V_{CC}) to the edge at which the output level swithches (0.5×VM)

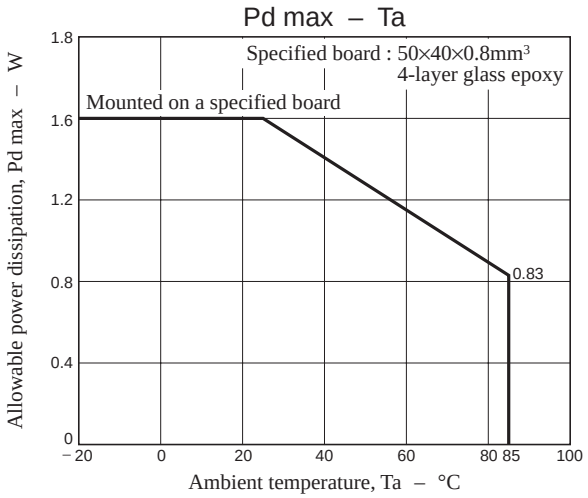
Note 2 : Output level switching time (VM transition time from 10 to 90 %)

Package Dimensions

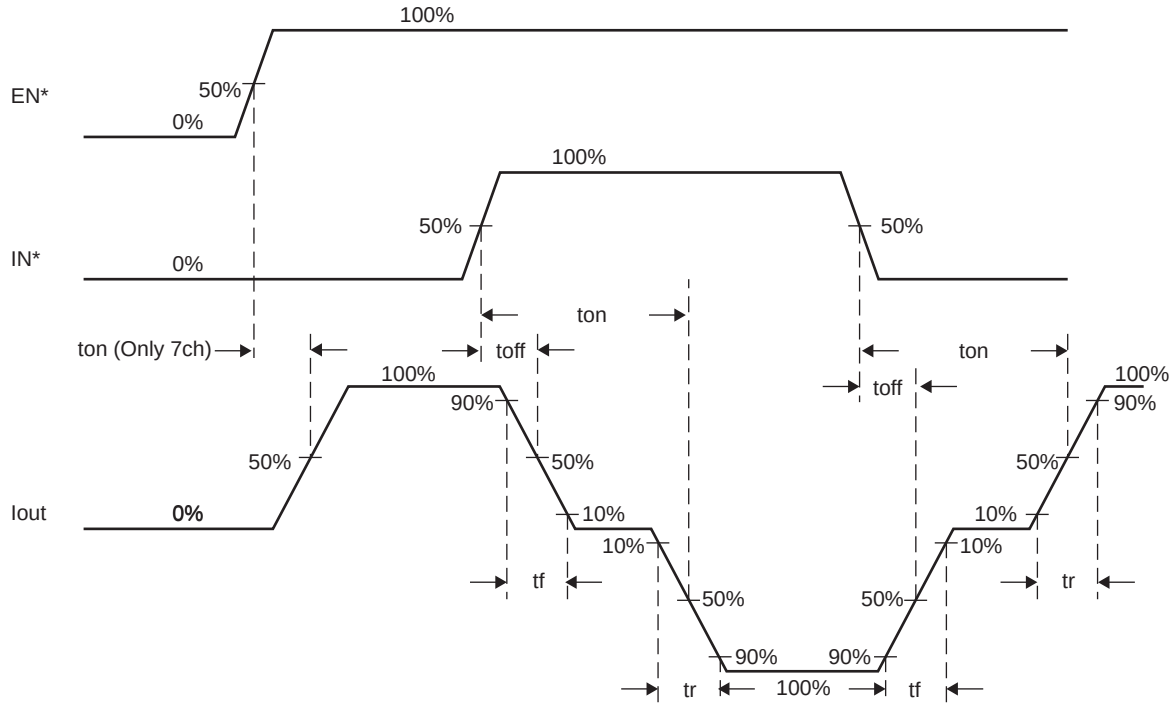
unit : mm (typ)

3363

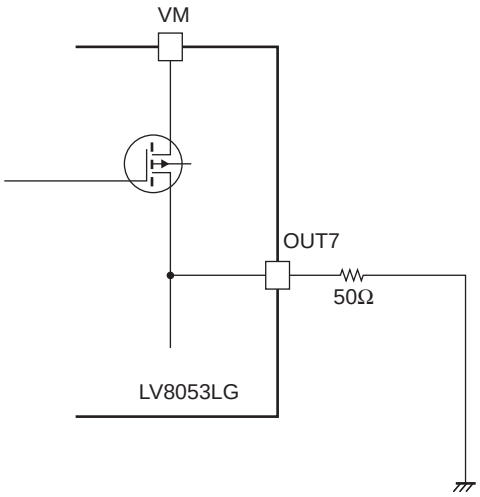




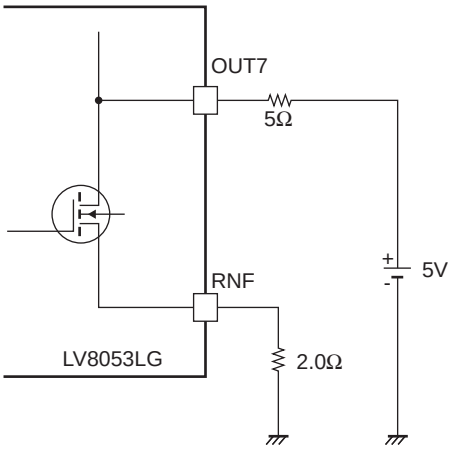
Switching Timing Chart



(Test circuit 1)

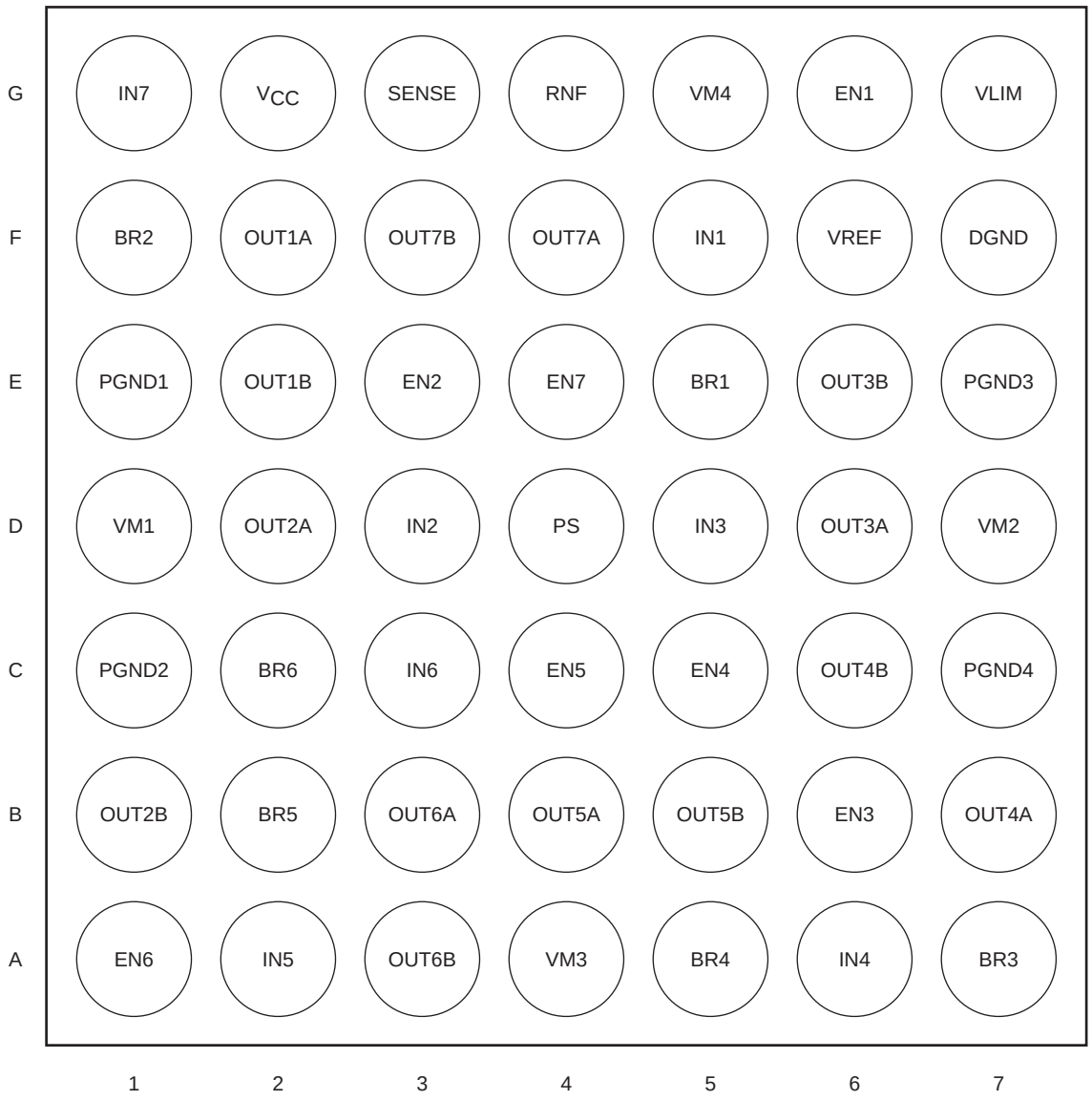


(Test circuit 2)



Pin Assignment

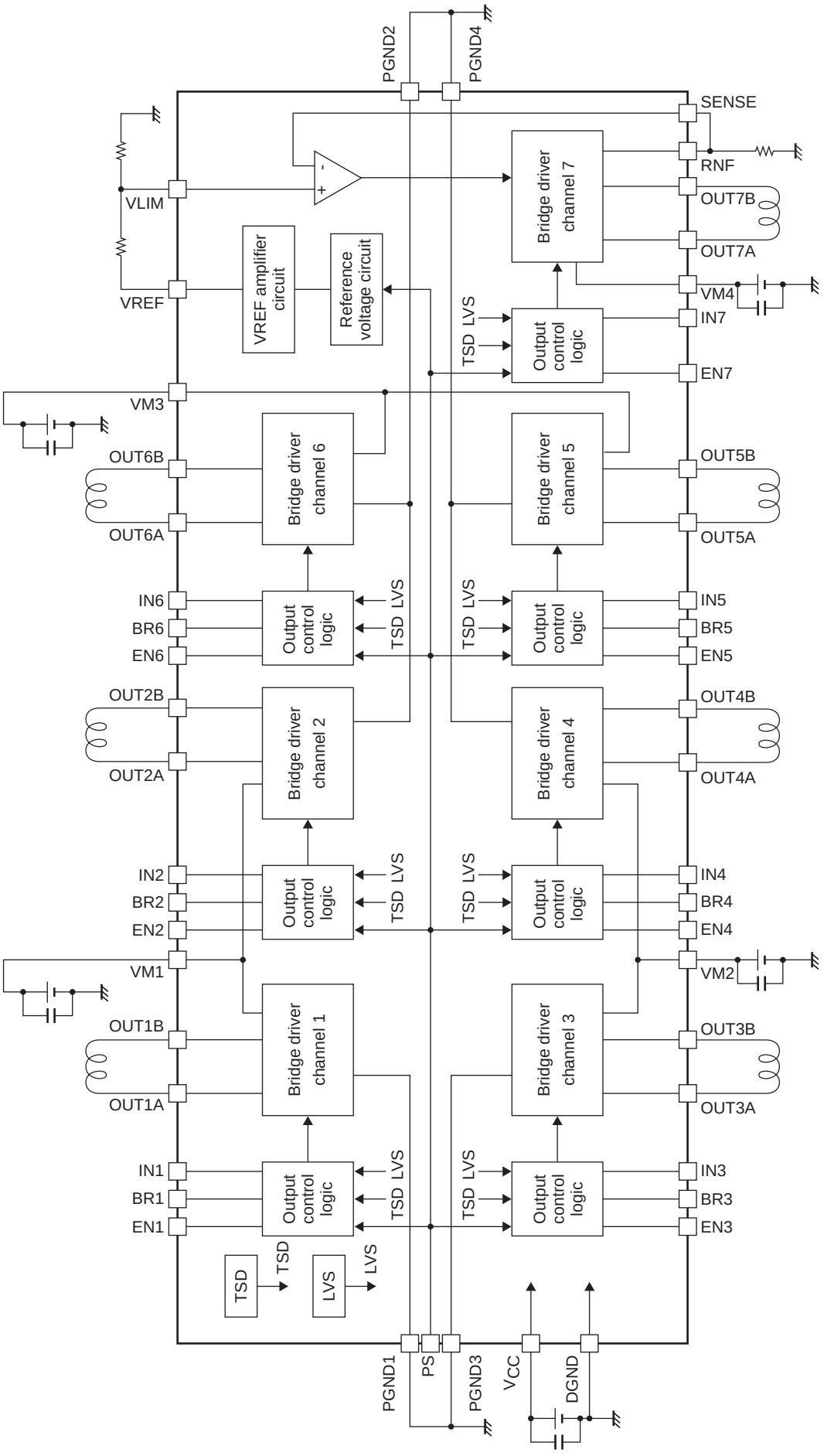
Bottom Veiw



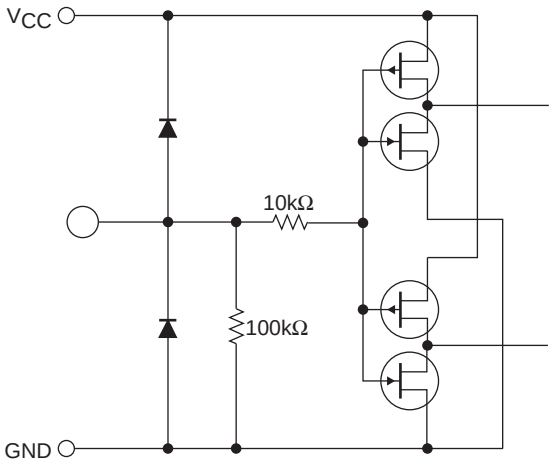
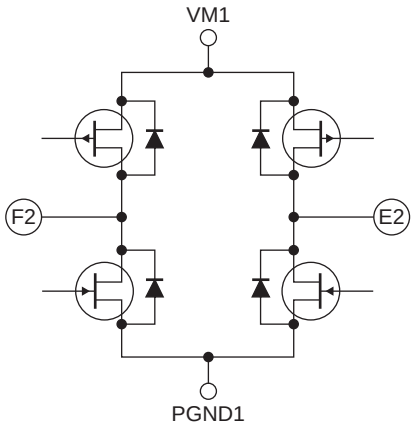
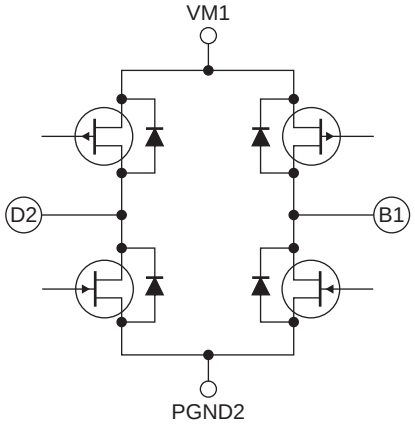
VM1 : 1-, 2-channel motor power supply
VM2 : 3-, 4-channel motor power supply
VM3 : 5-, 6-channel motor power supply
VM4 : 7-channel motor power supply

PGND1 : 1-channel power GND
PGND2 : 2-, 6-channel power GND
PGND3 : 3-channel power GND
PGND4 : 4-, 5-channel power GND

Block Diagram



Pin Functions

Pin No.	Pin Name	Pin Functtion	Equivalent Circuit
G2	V_{CC}	Control power supply	
D4	PS	Chip power save ON/OFF	
G6	EN1	Channel 1 motor power application pin	
E5	BR1	Channel 1 motor brake pin	
F5	IN1	Channel 1 forward/reverse control pin	
E3	EN2	Channel 2 motor power application pin	
F1	BR2	Channel 2 motor brake pin	
D3	IN2	Channel 2 forward/reverse control pin	
B6	EN3	Channel 3 motor power application pin	
A7	BR3	Channel 3 motor brake pin	
D5	IN3	Channel 3 forward/reverse control pin	
C5	EN4	Channel 4 motor power application pin	
A5	BR4	Channel 4 motor brake pin	
A6	IN4	Channel 4 forward/reverse control pin	
C4	EN5	Channel 5 motor power application pin	
B2	BR5	Channel 5 motor brake pin	
A2	IN5	Channel 5 forward/reverse control pin	
A1	EN6	Channel 6 motor power application pin	
C2	BR6	Channel 6 motor brake pin	
C3	IN6	Channel 6 forward/reverse control pin	
E4	EN7	Channel 7 motor power application pin	
G1	IN7	Channel 7 forward/reverse control pin	
F7	DGND	Control GND	
F2	OUT1A	Channel 1 OUTA output pin	
E2	OUT1B	Channel 1 OUTB output pin	
D2	OUT2A	Channel 2 OUTA output pin	
B1	OUT2B	Channel 2 OUTB output pin	

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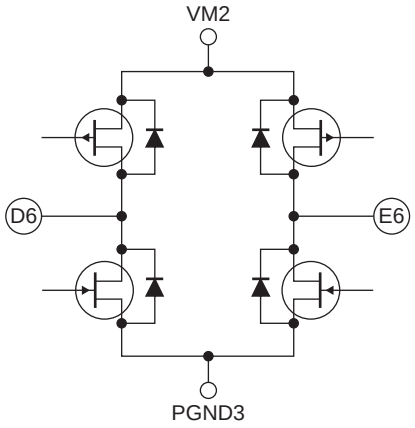
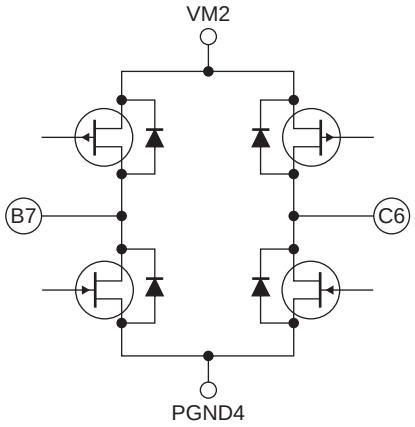
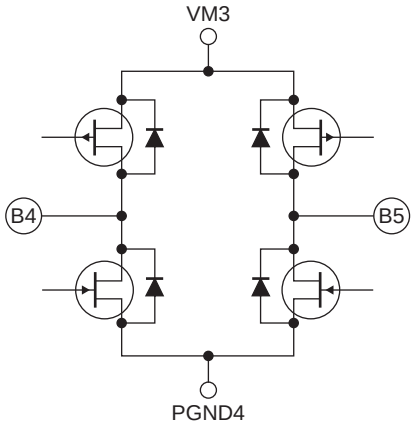
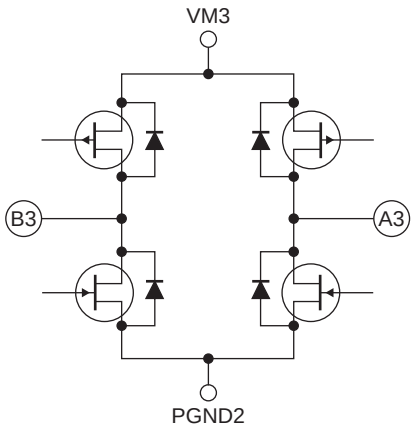
Pin No.	Pin Name	Pin Functtion	Equivalent Circuit
D6 E6	OUT3A OUT3B	Channel 3 OUTA output pin Channel 3 OUTB output pin	
B7 C6	OUT4A OUT4B	Channel 4 OUTA output pin Channel 4 OUTB output pin	
B4 B5	OUT5A OUT5B	Channel 5 OUTA output pin Channel 5 OUTB output pin	
B3 A3	OUT6A OUT6B	Channel 6 OUTA output pin Channel 6 OUTB output pin	

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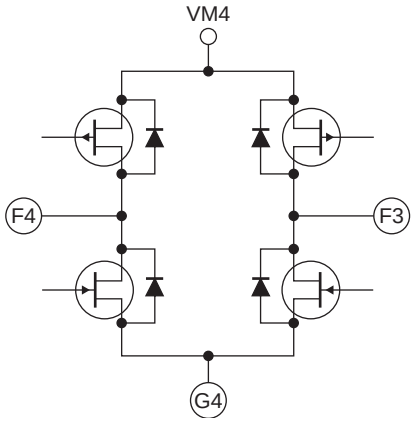
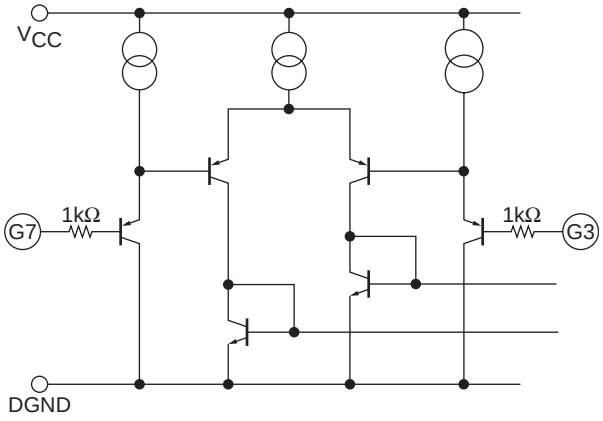
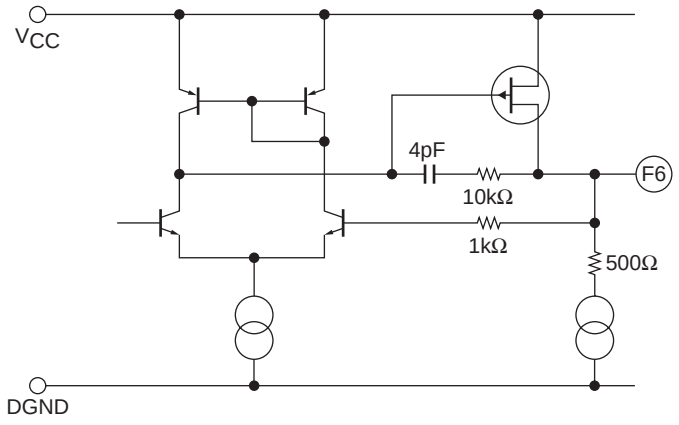
Pin No.	Pin Name	Pin Functtion	Equivalent Circuit
F4 F3 G4	OUT7A OUT7B RNF	Channel 6 OUTA output pin Channel 6 OUTB output pin Channel 7 current detection resistor connection pin	
D1 D7 A4 G5	VM1 VM2 VM3 VM4	Motor power supply (channel 1/channel 2) Motor power supply (channel 3/channel 4) Motor power supply (channel 5/channel 6) Motor power supply (channel 7)	
G7 G3	VLIM SENSE	Channel 7 reference voltage input pin Channel 7 current detection resistor connection pin	
F6	VREF	Channel 7 reference voltage output pin	
E1 C1 E7 C7	PGND1 PGND2 PGND3 PGND4	Power GND (channel 1) Power GND (channel 2/channel 6) Power GND (channel 3) Power GND (channel 4/channel 5)	

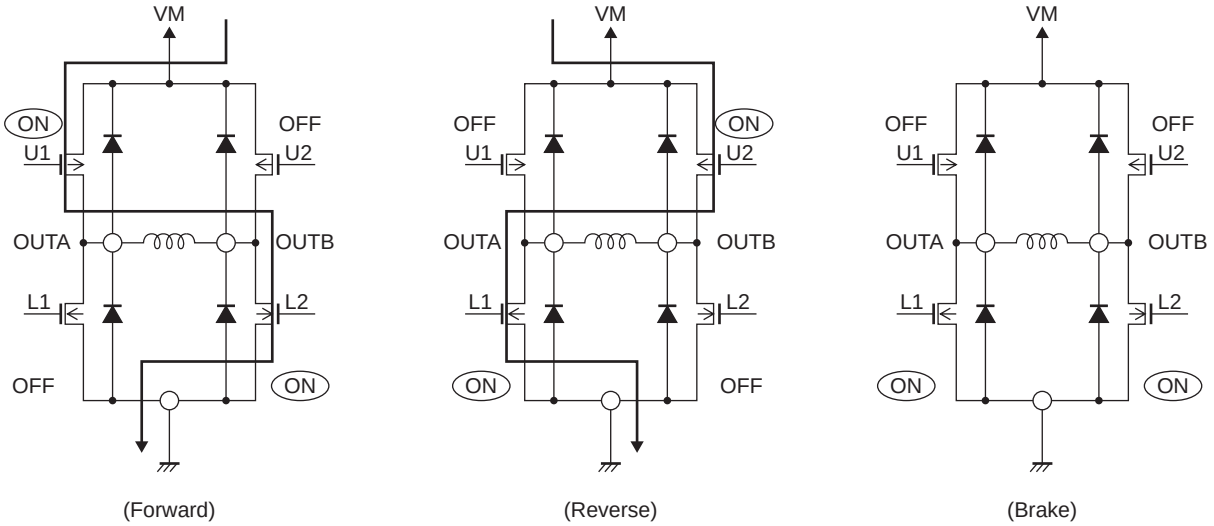
PWM drive forward/reverse motor driver (channels 1 to 6)

Logic input specifications (Common channels 1 to 6)

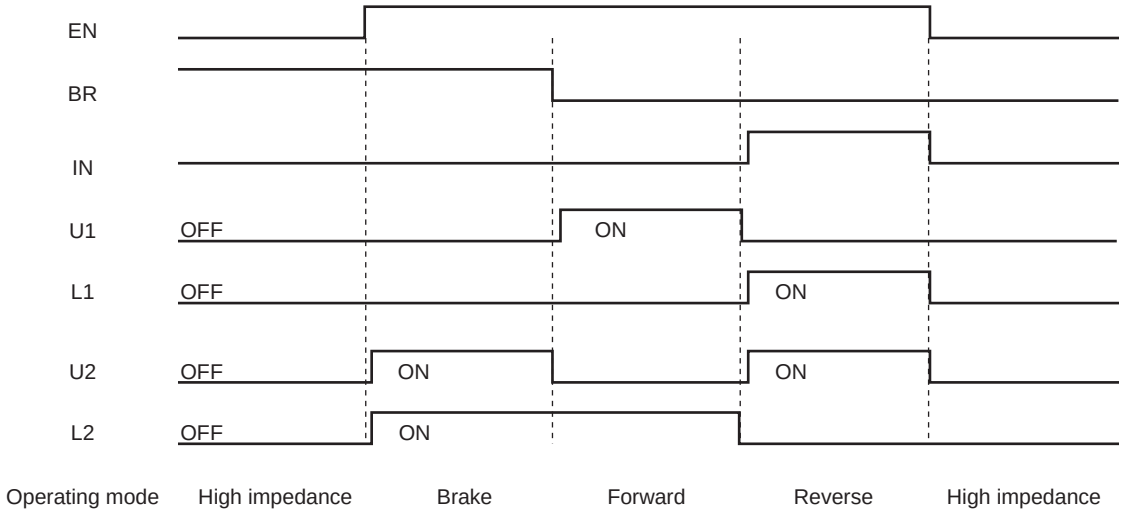
Input			Output		Operation mode
ENx	BRx	INx	OUTxA	OUTxB	
L	*	*	OFF	OFF	Standby
H	H	*	L	L	Brake
H	L	L	H	L	CW (forward)
H	L	H	L	H	CCW (reverse)

* : Don't care x : Channels 1 to 6

- Current limit control timing chart



Timing Chart

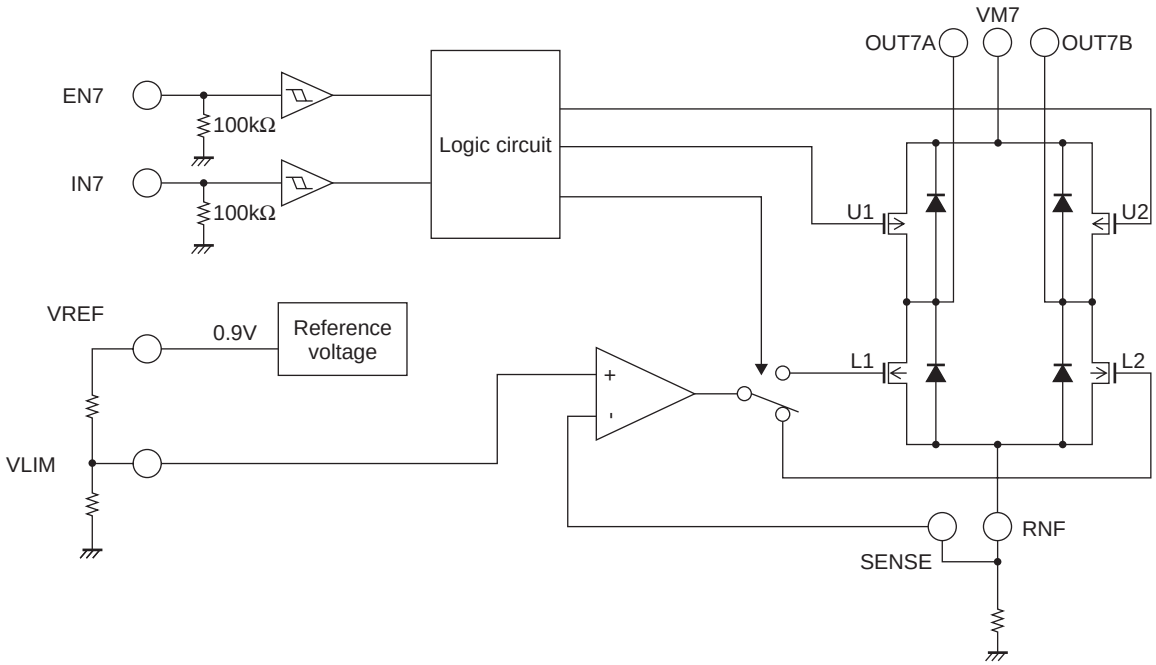


Constant current forward/reverse mortor driver (channel 7)

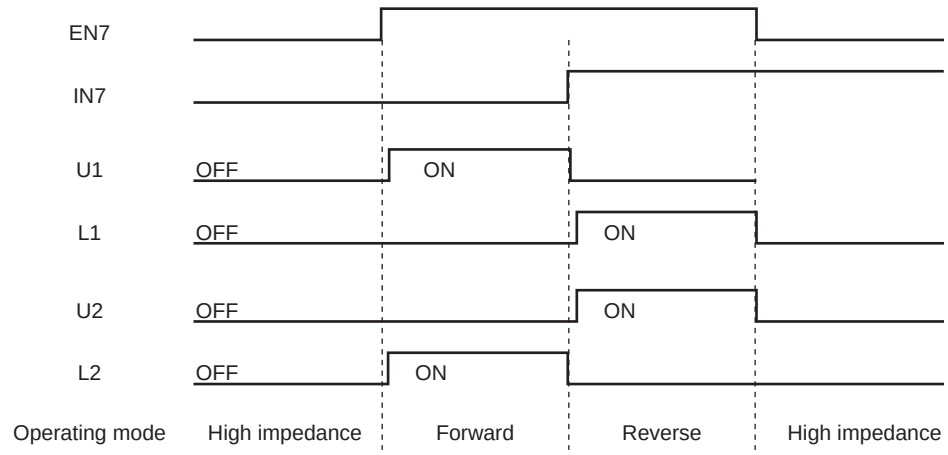
Truth table

Input		Output		Operation mode
EN7	IN7	OUT7A	OUT7B	
L	*	OFF	OFF	Standby
H	L	H	L	CW (forward)
H	H	L	H	CCW (reverse)

* : Don't care



Timing Chart



Procedure for calculating the set current

I_{OUT} = VLIM voltage / RNF resistance

Since the VLIM voltage is an external input, the reference voltage can be set arbitrarily.
A resistor divided voltage using the VREF pin (0.9V) can also be input to the VLIM pin.

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